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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,340	01/22/2004	Yen-Chang Chiu	MR2707-57	3276

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EXAMINER	
NGUYEN, TUAN HOANG	
ART UNIT	PAPER NUMBER
2618	
MAIL DATE	DELIVERY MODE
03/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,340	CHIU ET AL.	
	Examiner	Art Unit	
	TUAN H. NGUYEN	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *12,13 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 01/03/2008 with respect to claims 1-11, 14, and 16-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rofouragan et al. (U.S PUB. 2008/0045162 hereinafter “Rofouragan”) in view of Prockup (U.S PAT. 6,760,571) and further in view of Ishigaki (U.S PAT. 5,832,027).

Consider claim 1, Rofouragan teaches a single crystal oscillator RF transmitter system comprising: a microprocessor having a control signal output and a data output for output of digital data to be transmitted (page 5 [0109]); a local oscillator responsive to an external crystal for generating a first clock signal having a frequency in a radio

frequency band (page 6 [0118]); and the microprocessor, converter, local oscillator, clock switch and transmitter are integrated on a chip (page 4 [0102]).

Rofouragan does not explicitly show that a converter coupled to said microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system; and a transmitter connected to an output of the converter for receiving the digital packet data and being coupled to the local oscillator for use of the first clock signal as an RF carrier for the digital packet data to be transmitted by the transmitter.

In the same field of endeavor, Prockup teaches a converter coupled to said microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system (fig. 4 col. 4 lines 17-30); and a transmitter connected to an output of the converter for receiving the digital packet data and being coupled to the local oscillator for use of the first clock signal as an RF carrier for the digital packet data to be transmitted by the transmitter (fig. 4 col. 4 lines 17-30).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, a converter coupled to said microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system; and a transmitter connected to an output of the converter for receiving the digital packet data and being coupled to the local oscillator for use of the first clock signal as an RF carrier for the digital packet data to be transmitted by the transmitter, as taught by Prockup, in order to provide a

microprocessor obtains the difference of the counts in the counters, and from the difference computes the deviation of the modulated carrier from the center frequency of the carrier.

Rofouragan and Prockup, in combination, fail to teach a clock switch, coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter, the third clock signal being a different frequency than the first clock signal and the second clock signal, the clock switch having an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal.

However, Ishigaki teaches a clock switch, coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter, the third clock signal being a different frequency than the first clock signal and the second clock signal, the clock switch having an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal (col. 2 lines 1-38).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Ishigaki into view of Rofouragan and Prockup, in order to provide a frequency divider divides the frequency of the carrier by a predetermined integer N2. A spread code generator uses an output signal of the

frequency divider as a clock signal, and generates a spread code which is fed to the operation device.

Consider claim 2, Rofouragan further teaches the clock switch comprises a frequency divider for frequency-dividing the first clock signal to generate the second clock signal (page 6 [0119]).

Consider claim 3, Rofouragan further teaches the clock switch comprises a frequency divider for frequency-dividing the first clock signal to generate the third clock signal (page 6 [0120]).

Consider claim 14, Rofouragan teaches a method for transmitting data with an RF transmitter system having a single crystal oscillator and including a microprocessor connected with a converter that is in turn connected to a transmitter, the method comprising the steps of: generating a first clock signal at a radio frequency with a crystal oscillator for providing to the transmitter a carrier signal responsive to receipt of a control signal from the microprocessor to start generation of the first clock signal (page 5 [0109]).

Rofouragan does not explicitly show that converting digital data output from the microprocessor into digital packet data by the converter for output to the transmitter; and transmitting the digital packet data modulated on the first clock signal.

In the same field of endeavor, Prockup teaches converting digital data output from the microprocessor into digital packet data by the converter for output to the transmitter (fig. 4 col. 4 lines 17-30); and transmitting the digital packet data modulated on the first clock signal (fig. 4 col. 4 lines 17-30).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, converting digital data output from the microprocessor into digital packet data by the converter for output to the transmitter; and transmitting the digital packet data modulated on the first clock signal, as taught by Prockup, in order to provide a microprocessor obtains the difference of the counts in the counters, and from the difference computes the deviation of the modulated carrier from the center frequency of the carrier.

Rofouragan and Prockup, in combination, fail to teach generating a second clock signal and a third clock signal by dividing down the first clock signal for respectively providing to the microprocessor and converter clock signals of respectively reduced frequency.

However, Ishigaki teaches a clock switch, generating a second clock signal and a third clock signal by dividing down the first clock signal for respectively providing to the microprocessor and converter clock signals of respectively reduced frequency (col. 2 lines 1-38).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Ishigaki into view of Rofouragan and Prockup, in order to provide a frequency divider divides the frequency of the carrier by a

predetermined integer N2. A spread code generator uses an output signal of the frequency divider as a clock signal, and generates a spread code which is fed to the operation device.

4. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rofouragan in view of Prockup and Ishigaki further in view of Tian (U.S PAT. 6,624,710).

Consider claim 4, Rofouragan, Prockup and Ishigaki, in combination, fail to teach an RC oscillator for generating the second clock signal.

However, Tian teaches an RC oscillator for generating the second clock signal (col. 1 lines 26-37).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Tian into view of Rofouragan, Prockup and Ishigaki, in order to provide frequency of the output signal generated by the oscillator output signal is set as a function of a value of an included internal resistor integrated on the chip. An external resistor may be connected to the chip to allow a user to manipulate the oscillator output signal frequency.

Consider claim 5, Rofouragan further teaches the clock switch comprises a frequency divider for frequency-dividing the first clock signal to generate the third clock

signal (page 6 [0119]).

Consider claim 6, Tian further teaches the RC oscillator is connected with an external resistor for tuning the second clock signal (col. 1 lines 26-37).

Consider claim 7, Tian further teaches the external resistor comprises a variable resistor (col. 2 line 66 through col. 3 line 7).

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rofouragan in view of Prockup and Ishigaki and further in view of Yamazaki et al. (U.S PAT. 5,398,007 hereinafter "Yamazaki").

Consider claim 11, Rofouragan, Prockup and Ishigaki, in combination, fail to teach a peripheral circuit connected to the microprocessor.

However, Yamazaki teaches a peripheral circuit connected to the microprocessor (col. 7 lines 1-6).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Yamazaki into view of Rofouragan, Prockup and Ishigaki, in order to generate accurate baud rates for serial communication in a microcontroller running at a low system clock frequency, without restricting communication to low baud rates, drawing extra current and power, or requiring an extra external resonator.

6. Claims 8-10 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rofouragan in view of Prockup, Ishigaki and Tian, and further in view of Yamazaki.

Consider claim 8, Rofouragan, Prockup, Ishigaki, and Tian, in combination, fail to teaches the RC oscillator comprises a resistor network for determining the second clock signal.

However, Yamazaki teaches the RC oscillator comprises a resistor network for determining the second clock signal (fig. 6 col. 5 lines 49-59).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Yamazaki into view of Haban, Moriyama, and Tian, in order to generate accurate baud rates for serial communication in a microcontroller running at a low system clock frequency, without restricting communication to low baud rates, drawing extra current and power, or requiring an extra external resonator.

Consider claim 9, Yamazaki further teaches the microprocessor signals the local oscillator to turn off after the packets are transmitted (col. 5 lines 15-19).

Consider claim 10, Yamazaki further teaches the converter and transmitter signal the local oscillator to turn off after the packets are transmitted (col. 7 lines 1-6).

Consider claim 19, Yamazaki further teaches the step of trimming a built-in resistor network connected to the RC oscillator for determining the first clock (col. 5 lines 49-59).

Consider claim 20, Yamazaki further teaches the step of signaling the single crystal oscillator to stop generating the third clock after sending out the RF signal (col. 5 lines 15-19).

Consider claim 21, Yamazaki further teaches the step of signaling the converter to turn off after sending out the RF signal (col. 7 lines 1-6).

Consider claim 22, Yamazaki further teaches the step of signaling the transmitter to turn off after sending out the RF signal (col. 7 lines 1-6).

7. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rofouragan in view of Ishigaki and further in view of Tian (U.S PAT. 6,624,710).

Consider claim 16, Rofouragan teaches a method for transmitting data with an RF transmitter system having a single crystal oscillator and including a microprocessor connected with a converter that is in turn connected to a transmitter, the method comprising the steps of: generating a first clock signal at a radio frequency with a crystal

oscillator responsive to receipt of a control signal from the microprocessor to start generation of the first clock signal (page 5 [0109]); outputting digital data from the microprocessor for transmission by the transmitter (page 5 [0109]); and modulating the digital packet data with the first clock signal in the transmitter for transmitting an RF signal therefrom (page 4 [0106]).

Rofouragan does not explicitly show that generating a third clock signal from the first clock signal output from the crystal oscillator for coupling to converter, the third clock frequency being a lower frequency than a frequency of the first clock signal; generating a fourth clock signal from the second clock signal for coupling to the microprocessor, said fourth clock signal being a lower frequency than the frequency of the first clock signal and being a higher frequency than the third clock signal; converting the digital data output from the microprocessor into digital packet data by the converter.

In the same field of endeavor, Ishigaki teaches generating a third clock signal from the first clock signal output from the crystal oscillator for coupling to converter, the third clock frequency being a lower frequency than a frequency of the first clock signal (col. 2 lines 1-38); generating a fourth clock signal from the second clock signal for coupling to the microprocessor, said fourth clock signal being a lower frequency than the frequency of the first clock signal and being a higher frequency than the third clock signal (col. 2 lines 1-38); converting the digital data output from the microprocessor into digital packet data by the converter (col. 40 lines 19-23).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, generating a third clock signal from the first clock

signal output from the crystal oscillator for coupling to converter, the third clock frequency being a lower frequency than a frequency of the first clock signal; generating a fourth clock signal from the second clock signal for coupling to the microprocessor, said fourth clock signal being a lower frequency than the frequency of the first clock signal and being a higher frequency than the third clock signal; converting the digital data output from the microprocessor into digital packet data by the converter, as taught by Ishigaki, in order to provide a frequency divider divides the frequency of the carrier by a predetermined integer N2. A spread code generator uses an output signal of the frequency divider as a clock signal, and generates a spread code which is fed to the operation device.

Rofouragan and Ishigaki, in combination, fail to teach a clock switch, coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter, the third clock signal being a different frequency than the first clock signal and the second clock signal, the clock switch having an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal.

However, Ishigaki teaches a clock switch, coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter, the third clock signal being a different frequency than the first clock signal and the second clock signal, the clock switch having an input coupled to the control signal output of the microprocessor for

receiving a command therefrom to start the local oscillator to generate the first clock signal (col. 2 lines 1-38).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Ishigaki into view of Rofouragan and Prockup, in order to provide a frequency divider divides the frequency of the carrier by a predetermined integer N2. A spread code generator uses an output signal of the frequency divider as a clock signal, and generates a spread code which is fed to the operation device.

Rofouragan and Ishigaki, in combination, fail to teach generating a second clock signal using an RC oscillator.

However, Tian teaches generating a second clock signal using an RC oscillator (col. 1 lines 26-37).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Tian into view of Rofouragan and Ishigaki, in order to provide frequency of the output signal generated by the oscillator output signal is set as a function of a value of an included internal resistor integrated on the chip. An external resistor may be connected to the chip to allow a user to manipulate the oscillator output signal frequency.

Consider claim 17, Ishigaki further teaches the step of generating a fourth clock signal from the second clock signal comprises the step of frequency-dividing the second

clock signal (col. 2 lines 1-38).

Consider claim 18, Tian further teaches the step of tuning an external resistor connected to the RC oscillator for determining the first clock (col. 1 lines 26-37).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

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Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571)272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571)272-7882882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information Consider the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Nguyen
Examiner
Art Unit 2618

/Nay A. Maung/
Supervisory Patent Examiner, Art Unit 2618